image.

AF/2834

MS APPEAL BRIEF - PATENTS
PATENT
2565-0225P

IN THE U.S. PATENT AND TRADEMARK OFFICE

In re application of WADAKA, Shusou et al.

Before the Board of Appeals

Appeal No.:

Appl. No.:	09/778,872	Group:	2834
Filed:	February 8, 2001	Examiner:	M. Budd
Conf.:	9099		

For: FILM ACOUSTIC WAVE DEVICE AND ITS MANUFACTURING METHOD AND CIRCUIT DEVICE

REPLY BRIEF TRANSMITTAL FORM

MS APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

November 12, 2003

Sir:

Transmitted herewith is a Reply Brief (in triplicate) on behalf of the appellants in connection with the above-identified application.

☒ The enclosed document is being transmitted via the Certificate of Mailing provisions of 37 C.F.R. § 1.8.

The Examiner's Answer was mailed on September 11, 2003.

☐ An extension of time under 37 C.F.R. § 1.136(b) to was requested on and was approved on .

☐ Please charge Deposit Account No. 02-2448 in the amount of $0.00. A triplicate copy of this sheet is attached.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

BIRCH, STEWART, KOLASCH & BIRCH, LLP

By _____
Michael K. Mutter, #29,680

RWD

MKM/RWD/mzk
2565-0225P

Attachment(s)

P.O. Box 747
Falls Church, VA 22040-0747
(703) 205-8000

(Rev. 09/30/03)

MS APPEAL BRIEF - PATENTS
PATENT
2565-0225P

IN THE U.S. PATENT AND TRADEMARK OFFICE

In re application of		Before the Board of Appeals	
WADAKA, Shusou et al.		Appeal No.:	
Appl. No.:	09/778,872	Group:	2834
Filed:	February 8, 2001	Examiner:	M. Budd
Conf.:	9099		
For:	FILM ACOUSTIC WAVE DEVICE AND ITS MANUFACTURING METHOD AND CIRCUIT DEVICE		

REPLY BRIEF

MS APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

November 12, 2003

Sir:

In response to the Examiner's Answer of September 11, 2003, the following remarks are respectfully submitted.

The Examiner's Answer did not specifically indicate a period to reply. Applicants submit this Reply Brief within the usual period for replying to Examiner's Answers of two months.

Appellants submit that new arguments have been presented that necessitate this Reply Brief, and submit that the arguments made in this Reply Brief are proper. Specifically, the Examiner's Answer has for the first time pointed out the specific teachings of each reference in support of his rejections, particularly the 35 U.S.C. 102 rejection. For example, the Examiner's Answer states for the first time that various substrates (e.g., Krishnasawamy's substrate 57) constitute the claimed wafer.

Each of the substrates in Krishnasawamy fail to teach the claimed wafer and none of the references relied on address the problem solved by the present claimed invention. None of the substrates indicated in the Examiner's Answer can be considered a "wafer" within the usual meaning of the term as defined in the semiconductor manufacturing art.

Appellants submit that the terms "wafer" and "substrate" are terms of art with distinct meanings. Wafer technology is a well know approach to cost efficient fabrication of a large number of VLSI chips, and a wafer is an intermediate component used in that fabrication process. Wafers are typically range in diameter from 100 to 300mm.

Background for the term "wafer"

A typical microelectronic fabrication process begins with the growth of a crystal of semiconductor material, e.g., silicon or gallium arsenide, having the diameter of 100mm to 300mm. The crystal is then sliced into wafers (per the common usage of wafer in the phrase, "to divide into wafers"). Layers of

material are added to the wafer via masks, diffusion, implantation, etc. The final wafer contains a number of dies that are the circuit being produced for a particular application. A wafer consists of a large number of potential sites. The yield of a wafer then constitutes the number of good dies produced out of the total number of potential sites. It is well known in the art that the smaller the die size, the larger the yield. Thus, a wafer typically results in a number of good dies being produced.

Present Invention

The present application relies on the usual meaning of the term "wafer" within the art of microelectronic fabrication. In particular, with respect to Figure 1, the present specification states, "Since a several number of the film acoustic wave devices 12a~12c are arranged on top of the single wafer 11, much number of the film acoustic wave devices 12 can be manufactured at once from a processing of the single wafer 11." Further, it is disclosed that a wafer is conventionally used to manufacture a plurality of devices at once, e.g., 100 or more devices (Specification at page 26, lines 15-16). And still further, the present specification states, "The greater the number of film acoustic wave devices 12 obtained from the single wafer, the cost of manufacturing per film acoustic wave device 12 becomes low." (Specification, paragraph bridging pages 26-27)

Differences over Krishnaswamy

None of the references of record explicitly disclose wafer(s), much less wafers having the claimed characteristics. Inherency is not an issue presented in the rejections of record. Therefore, Appellants submit that each of rejections made in the Final Office Action fail to establish *prima facie* anticipation of the claimed invention.

The Examiner's Answer states that Krishnasawamy's substrate 57 teaches the claimed wafer. However, Krishnasawamy's substrate does not meet the usual meaning of "wafer". Rather, Krishnaswamy is concerned with a single chip. Such a single chip may not be considered a wafer for the reasons expressed above. Krishnasawamy is completely silent with respect to the term "wafer" and use of wafer technology in a fabrication process.

Because Krishnaswamy does not disclose a wafer and fabrication using wafer technology, it does not address the problem solved by the present invention. Unlike Krishnaswamy, the present claimed invention is directed to a wafer having a plurality of acoustic wave devices, and among other things, "wherein at least one component in some of the plurality of acoustical wave devices is modified in its operational characteristic to compensate for the variation in the at least one characteristic of the piezoelectric thin film and is based on the location of the at least one acoustical wave device on the wafer." In other words, Krishnaswamy fails to teach a wafer having the claimed structural characteristics.

Accordingly, Appellants submit that Krishnaswamy does not teach or suggest each and every claimed element.

Differ nces ver other References

The Examiner's Answer likewise states that the claimed wafer is taught by Corran #24, Berlincourt #12, Vale #30, and JP '804 #3. As with Krishnaswamy, each of those references is merely concerned with a substrate for a single chip and are completely silent with respect to a wafer. Accordingly, Appellants submit that none of the references relied on in the Final Office Action teach the claimed wafer and address the problem solved by the present claimed invention.

Therefore, for at least these and reasons set forth in the Appeal Brief, Appellants respectfully request that all rejections based on prior art of record be withdrawn.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. 1.16 or under 37 C.F.R. 1.17; particularly, extension of time fees.

Respectfully submitted,

BIRCH STEWART KOLASCH & BIRCH, LLP

By:_____
Michael K. Mutter
Registration No. 29,680

MKM/RWD/mzk
2565-0225P

P.O. Box 747
Falls Church, VA 22040-0747
(703) 205-8000